Session 28 Overview

Image Sensors

Chair: Johannes Solhusvik, *Micron Technology, Oslo, Norway*

Associate Chair: Hirofumi Sumi, *Sony, Tokyo, Japan*

CMOS image sensors are now the undisputed technology of choice for most consumer imaging applications including camcorders and digital still cameras (DSCs). CMOS image sensors offer lower cost, lower size and lower power than CCDs without compromising on performance.

The constant drive for improved image quality and target extraction leads to continued innovation in multiple-resolution image sensors in both the spatial and temporal domains for both infrared and fluorescence imaging. Innovations are presented in the area of on-chip processing, both inside and outside the pixel array.

The push for lower cost motivates both innovations in pixel design to reduce die size and advanced optics to compensate for non-uniformities and color shading artifacts. These artifacts are associated with small-pixel image sensors and optics with wide angles of incidence.

Paper 28.1 from ARC Seibersdorf Research describes the first line sensor to combine an asynchronous, data-driven pixel circuit with on-chip sub-microsecond time-stamping and a synchronous bus-arbiter. The asynchronous operation reduces the data output rate by orders of magnitude.

The authors of Paper 28.2 from U Minnesota, Pixelplus, and KAIST describe an image sensor capable of automatically detecting fast moving objects in the scene. The region-of-interest associated with the object can then be read out at up to 960 frames per second. This rate is much higher than the rest of the image, which is typically read out at 30 frames per second.

In certain imaging applications, such as infrared imaging and fluorescence imaging, the challenge is to extract the scene contrast in the presence of a very large background signal level. Paper 28.3 from Stanford presents an excellent technique for subtracting the background signal in such situations.

Image sensors designed for high-speed readout often use one ADC per column, with the ADCs operating in parallel to achieve the desired frame rate. Paper 28.4 from TU Delft and DALSA describes a CMOS image sensor that uses a column-parallel ADC with a new multiple-ramp single-slope architecture. It achieves a 3.3× reduction in ADC conversion time compared to classical single-slope ADCs with only a 24% increase in power consumption.

Paper 28.5 from Micron Technology presents the first 8.1Mpixel CMOS image sensor product that features 1.75×1.75μm^2 pixels intended for consumer applications such as DSCs and cell phones using the 1/2.5 inch optical format. This format typically uses 3Mpixel and 5Mpixel sensors today. The sensor yields 63.8dB dynamic range and an impressively low noise floor of 3.8e^-_{rms}.

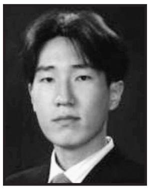
Paper 28.6 from Canon describes a 1/2.7 inch high-definition (HD) CMOS image sensor. This sensor uses low-noise readout circuitry and optimized pixel design to achieve an impressive 3.7e^-_{rms} noise floor and 12.2e^-/s dark current at 60°C.

Paper 28.7 from Grass Valley and Thomson Silicon Components presents a 2/3 inch HD CMOS image sensor. It offers a wide selection …1080p. The authors of Paper 28.8 conclude the session by describing a MOS image sensor with digital microlenses to increase the sensitivity on the periphery of the imager so that uniform brightness is achieved even with an angle of incidence >45°.

28.1 A Dual-Line Optical-Transient Sensor with On-Chip Precision Time-Stamp Generation **1:30 PM**

C. Posch, ARC Seibersdorf Research, Vienna, Austria

A 120dB dynamic range 2×256 dual-line optical transient sensor uses pixels that respond asynchronously to relative intensity changes. A time stamp with variable resolution down to 100ns is allocated to the events at the pixel level. The pixel address and time stamp are read out via a 3-stage pipelined synchronous arbiter. The chip is fabricated in 0.35μm CMOS, runs at 40MHz and consumes 250mW at 3.3V.



28.2 A Spatial-Temporal Multi-Resolution CMOS Image Sensor with Adaptive Frame Rates for Moving Objects in the Region-of-Interest **2:00 PM**

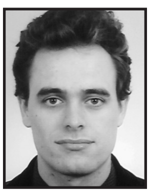
J. Choi, University of Minnesota, Minneapolis, MN

A CMOS image sensor simultaneously generates spatial-temporal multi-resolution images from two channels: one for normal images (<30fps) for stationary backgrounds; and the other for high-frame-rate images (adaptable to over 960fps) with reduced spatial resolution for moving objects in the region-of-interest. This sensor employs on-chip motion detection circuits, consumes 75mW at 3.3V and is fabricated in 0.35μm CMOS.

28.3 A Per-Pixel Pulse-FM Background Subtraction Circuit with 175ppm Accuracy for Imaging Applications **2:30 PM**

S. Kavusi, Stanford University, Stanford, CA

A per-pixel background subtraction circuit for infrared and fluorescence imaging applications is presented. Charge packets controlled by a pulse-FM signal are subtracted from the integrator of each pixel. A 1×16 array of 30μm pixels prototyped in a 0.18μm CMOS process achieves noise, linearity, and spatial current variation of 175ppm, 270ppm, and 3%, respectively, at 43fps.



28.4 A CMOS Image Sensor with a Column-Level Multiple-Ramp Single-Slope ADC **3:15 PM**

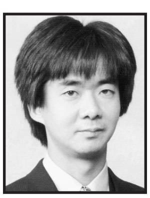
M. Snoeij, Delft University of Technology, Delft, The Netherlands

A CMOS image sensor uses a column-level ADC with a multiple-ramp single-slope (MRSS) architecture. This architecture has a 3.3× shorter conversion time than a classic single-slope architecture with equal power. Like the single-slope ADC, the MRSS ADC requires a single comparator per column, and, additionally, 8 switches and some digital circuitry. A prototype in a 0.25μm CMOS process has a frame rate 2.8× that of a single-slope ADC while dissipating 24% more power.

28.5 A 1/2.5 inch 8.1Mpixel CMOS Image Sensor for Digital Cameras **3:45 PM**

K-B. Cho, Micron Technology, Pasadena, CA

A 1/2.5 inch 8.1Mpixel CMOS image sensor with 1.75μm pixel pitch is designed to operate at 2.8V for digital still camera applications and down to 2.4V in mobile applications. The chip uses top and bottom multiple channels with a double-data-rate analog signal readout at a rate of 96Mpixels/s, which results in total 192Mpixels/s. With the analog gain set to 15.875 and a 12b ADC the noise floor falls as low as $3.8e^-$, yielding a pixel DR of 63.8dB.



28.6 A 1/2.7 inch Low-Noise CMOS Image Sensor for Full HD Camcorders **4:15 PM**

H. Takahashi, Canon, Ayase, Japan

A 1/2.7 inch 1944×1092pixels CMOS image sensor with multi-gain column amplifier and double noise canceller is fabricated in a 0.18μm 1P3M CMOS process. It operates at 48MHz in a progressive scanning mode at 60fps. A 2T/pixel architecture and low optical stack with micro innerlens achieve $14.8ke^-$/lx-s sensitivity, $14ke^-$ saturation, $3.7e^-_{rms}$ noise and $12.2e^-$ dark current at 60°C.

28.7 A 2/3 inch CMOS Image Sensor for HDTV Applications with Multiple High-DR Modes and Flexible Scanning **4:45 PM**

P. Centen, Grass Valley, Breda, The Netherlands

A 3T CMOS image sensor is designed with cost-effectiveness and a high degree of flexibility in mind. It supports an optimal interaction between imager and the external processing. An overall noise level of $11.5e^-$ ($4e^-$ for the pixel alone) is obtained along with a Q_{max} of more than $15ke^-$ per pixel. The design supports 1920(H)×1080(V)p90 and 1920(H)×1080(V)i180 at a data rate of 2.7Gb/s.

28.8 A MOS Image Sensor with Microlenses Built by Sub-Wavelength Patterning **5:00 PM**

K. Toshikiyo, Matsushita Electric Industrial, Kyoto, Japan

A MOS image sensor has digital-microlenses implemented by sub-wavelength patterning of concentric SiO_2 ring walls. The sensitivity at the periphery of the imager is $3000e^-$/lx-s. In comparison, the sensitivity at the periphery of a conventional imager is $1300e^-$/lx-s. Thus, extremely uniform brightness throughout the reproduced image is demonstrated even with an angle of incidence >45°.